## REMARKS

This application is under final rejection. Applicant has presented arguments herein below that Applicant believes should render the claims allowable. In the event, however, that the Examiner is not persuaded by Applicant's arguments, Applicant respectfully requests that the Examiner enter the amendment to clarify issues upon appeal.

These remarks are responsive to the Office Action dated April 2, 2002. Claims 9-16 are pending in the present Application. Claims 9-16 are rejected. Claims 9-16 remain pending. For the reasons set forth more fully below, Applicant respectfully submits that the remaining claims are allowable. Consequently, reconsideration, allowance and passage to issue are respectfully requested.

The present invention comprises a system for forming a channel device. The system comprises means for providing an active region on a substrate wherein the active region comprises a plurality of discontinuous gate structures. The system further comprises means for providing an ion implantation in the substrate.

***35 USC §102 Rejections***

For ease of review, independent claim 9 is reproduced herein below:

9. A system for forming a channel device comprising:

means for providing an active region on a substrate wherein the active region comprises a plurality of discontinuous gate structures; and

means for providing an ion implantation in the substrate.

The Examiner states:

> **Claims 9, 10, 11, 13, 14, 15 and 16 are rejected under 35 USC 102(b) as being anticipated by Dennison et al. (US '854).**
>
> **Dennison teaches a system forming a channel device comprising (see figures 1-5 and col. 2, line 15 to col. 5, line 25:**
>
> **means for providing one active region comprises three gate structures 16, 20, 24 on a substrate 12; and**
>
> **means for providing an ion implantation in the substrate, wherein means for providing the ion implantation further comprises means 38 for masking the gate structure before the ion implantation and wherein the ion implantation further comprises a halo or pocket 44 implant and wherein the gate structures are inherently connected to gate voltage source.**

Applicant respectfully disagrees with the Examiner's rejection. The recited invention of claim 9 is directed toward a system for forming a channel device. The system comprises means for providing an active region on a substrate wherein the active region comprises a plurality of discontinuous gate structures. The system further comprises means for providing an ion implantation in the substrate.

Dennison discloses a method of forming CMOS integrated circuitry includes, providing a series of gate lines over a semiconductor substrate, a first gate line being positioned relative to an area of the substrate for formation of an NMOS transistor, a second gate line being positioned relative to an area of the substrate for formation of a PMOS transistor. The method further includes masking the second gate line and the PMOS substrate area while conducting a p-type halo ion implant into the NMOS substrate area adjacent the first gate line, the p-type halo ion implant being conducted at a first energy level to provide a p-type first impurity concentration at a first depth within the NMOS substrate area.

Finally, phosphorus is implanted into both the NMOS substrate area and the PMOS substrate area adjacent to the first and the second gate lines to form both NMOS LDD regions and PMOS n-type halo regions.

The Examiner asserts that Dennison anticipates the present invention because it teaches a system for forming a channel device comprising means for provide one active region and three gate structures 16, 20, 24 on a substrate 12. (See Dennison, Figure 1, Attached Exhibit A.) Applicant **has previously** argued in Amendment dated 1/17/02 that the plurality of gate structures 16, 20, 24 are on three **different** active regions **a, b, c.** (i.e. gate structure 16 is on active region **a**, gate structure 20 is on active region **b**, gate structure 24 is on active region **c**.). In response to the Applicant's amendment, the Examiner submits that the single substrate 12 in Figure 1 constitutes a single active region. Applicant disagrees with this assessment.

The present invention of claim 9 recites an active region on a substrate wherein the active region comprises a plurality of discontinuous gate structures. For the purposes of the Applicant's above referenced patent application, active regions are regions that are defined on the substrate via a LOCOS (Local Oxidation of Silicon) or similar process, upon which gates stacks are formed. These active regions are separated by isolation regions that are typically formed by growing a thin field oxide region (FOX) between the active regions using a thermal oxidation process. As a result, a plurality of active regions are formed on a single substrate.

Item 12 of Figure 1 comprises a bulk silicon substrate upon which **a plurality of** active regions 18, 22, 26 are formed, not a single active region. Therefore, Dennison discloses a series of gate structures 16, 20, 24 wherein each gate structure is on a separate

active region on a bulk silicon substrate 12 (i.e. gate structure 16 is on active region 18, gate structure 20 is on active region 22, gate structure 24 is on active region 26). Referring now to Figure 5 of the above-referenced patent application (see attached Exhibit B), a single active region is shown wherein the active region comprises a plurality of discontinuous gate structures 204. Applicant accordingly asserts that a series of gate structures, wherein each gate structure in the series of gate structures is on a separate active region on a bulk silicon substrate, **as shown in the cited art** is clearly different from a plurality of discontinuous gate structures, wherein the plurality of discontinuous gate structures is on a single active region **as recited in the present invention**

Consequently, the recited invention of claim 9 is clearly different from the cited reference. Accordingly, claim 9 is allowable over the cited reference.

Since claims 10, 11, 13, 14, 15 and 16 are dependent on claims 9, the above-articulated arguments related to claim 9 apply with equal force to claims 10, 11, 13, 14, 15 and 16. Accordingly, claims 10, 11, 13, 14, 15 and 16 are allowable over the cited reference.

***35 USC §103 Rejections***

The Examiner states:

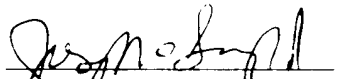
> **Claim 12 is rejected under 35 USC 103(a) as being unpatentable over Dennison et al. (US '854) as applied to claims 9, 10, 11, 13, 14, 15 and 16 above, and further in view of the following remarks.**
>
> **Dennison teaches each of the three gate structures comprises a channel length and disposed at a distance apart, but fails to teach the range for the channel length and separated distance as recited in present claim 12.**
>
> **However, it would have been obvious to one of ordinary skill in the art of making semiconductor devices to determine the workable or optimal range for the channel length and separated distance through routine**

**experimentation and optimization to obtain optimal or desired device performance.**

Since claim 12 is dependent on claim 9, the above-articulated arguments related to claim 9 apply with equal force to claim 12. Accordingly, claim 12 is allowable over the cited reference.

Applicant believes that this application is in condition for allowance. Accordingly, Applicant respectfully requests reconsideration, allowance and passage to issue of claims 9-16 as now presented. Should any unresolved issue remain, Examiner is invited to call Applicant's attorney at the telephone number indicated below.

Respectfully submitted,



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